

What is claimed is:

- 1 1. A circuit for a pixel site in an imaging array, comprising:
2 a pixel to convert incident light to an electrical signal;
3 a row line to read out a voltage from said pixel;
4 a row line transistor, operatively connected between one end of said row line and
5 a predetermined voltage, to reset a voltage associated with said row line; and
6 a reset voltage generator, operatively connected to said row line transistor, to
7 generate reset pulses;
8 said reset voltage generator generating a first reset pulse at a beginning of an
9 integration period of said pixel;
10 said reset voltage generator generating a second reset pulse after generating said
11 first reset pulse, the generation of the second reset pulse being at an end of the integration
12 period of said pixel.

- 1 2. The circuit as claimed in claim 1, wherein said pixel comprising:
2 a light-detecting element to convert incident light to a photocurrent;
3 a reset transistor, operatively connected to said light-detecting element, to reset a
4 voltage associated with said light-detecting element; and
5 a pixel reset voltage generator, operatively connected to a non-gate terminal of
6 said reset transistor, to generate a reset voltage;
7 said pixel reset voltage generator generating a first pixel reset voltage;
8 said pixel reset voltage generator generating a second pixel reset voltage after
9 generating said first pixel reset voltage.

- 1 3. The circuit as claimed in claim 1, wherein said predetermined voltage is
2 ground.

- 1 4. The circuit as claimed in claim 2, wherein said pixel further comprising:
2 a transistor;
3 said transistor having a gate thereof operatively connected to said light-detecting
4 element;

5 said transistor having a non-gate terminal thereof operatively connected to said
6 pixel reset voltage generator.

1 5. The circuit as claimed in claim 2, wherein said pixel further comprising:
2 a transistor;

3 said transistor having a gate thereof operatively connected to said light-detecting
4 element;

5 said transistor having a non-gate terminal thereof operatively connected to a
6 voltage source.

1 6. The circuit as claimed in claim 2, wherein said first pixel reset voltage has a
2 value to drive said reset transistor to operate in a triode region.

1 7. A method for measuring a pixel voltage using a row line, comprising:
2 (a) hard resetting the row line voltage to a first predetermined voltage;
3 (b) soft resetting the row line voltage to a first pixel voltage;
4 (c) hard resetting the row line voltage to a second predetermined voltage;
5 (d) soft resetting the row line voltage to a second pixel voltage; and
6 (e) determining a difference between the first and second pixel voltages, the
7 difference being the measured pixel voltage.

1 8. The method as claimed in claim 7, wherein the first predetermined voltage is
2 equal to the second predetermined voltage.

1 9. The method as claimed in claim 7, wherein the first predetermined voltage is
2 ground.

1 10. The method as claimed in claim 7, wherein the second predetermined voltage
2 is ground.

1 11. The method as claimed in claim 7, wherein the first and second
2 predetermined voltages are ground.

1 12. The method as claimed in claim 7, wherein the first pixel voltage is a pixel
2 reset voltage and the second pixel voltage is a pixel integrated voltage.

1 13. The method as claimed in claim 7, wherein the second pixel voltage is a pixel
2 reset voltage and the first pixel voltage is a pixel integrated voltage.

1 14. The method as claimed in claim 7, further comprising:
2 (f) generating a hard reset of a voltage associated with a light-detecting element of
3 the pixel to reset the voltage associated with the light-detecting element; and
4 (g) generating a soft reset of the voltage associated with the light-detecting
5 element, after generating the hard reset, to reset the voltage associated with the light-
6 detecting element.

1 15. A method for measuring a pixel voltage using a row line, the row line
2 including a row line transistor, comprising:

3 (a) turning ON the row line transistor to bring the row line to a first predetermined
4 voltage level;
5 (b) turning ON a column select transistor associated with the pixel and turning
6 OFF row line transistor to bring the row line voltage up to a pixel voltage level;
7 (c) capturing a first voltage value on the row line;
8 (d) turning ON the row line transistor to bring the row line to a second
9 predetermined voltage level;
10 (e) turning ON a column select transistor associated with the pixel and turning
11 OFF row line transistor to bring the row line voltage up to a pixel voltage level;
12 (f) capturing a second voltage value on the row line; and
13 (g) determining a difference between the first and second captured voltage values,
14 the difference being the measured pixel voltage.

1 16. The method as claimed in claim 15, wherein the first predetermined voltage is
2 equal to the second predetermined voltage.

1 17. The method as claimed in claim 15, wherein the first predetermined voltage is
2 ground.

1 18. The method as claimed in claim 15, wherein the second predetermined
2 voltage is ground.

1 19. The method as claimed in claim 15, wherein the first and second
2 predetermined voltages are ground.

1 20. The method as claimed in 15, wherein the first voltage value is a pixel reset
2 voltage and the second voltage value is a pixel integrated voltage.

1 21. The method as claimed in 15, wherein the second voltage value is a pixel
2 reset voltage and the first voltage value is a pixel integrated voltage.